

Recovery method to mitigate the effect of NBTI on SRAM cells

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ABSTRACT

NBTI stands for Negative Bias Temperature Instability. NBTI basically affects the parameter at the device level and hence affects the performance of the device. This paper explains what NBTI is and its effect on the SRAM cells while also dealing with the leakage current that is supposed to be one of the important factors affecting any circuit. Not just that but this paper also puts forth a method called recovery mode which explains a different approach to overcome this effect of NBTI on the 6T SRAM cell.

Index Terms: 6T SRAM cell, leakage current, NBTI.

I. INTRODUCTION

Memories today, play an important role and have benchmarked their significance in the field of digital VLSI over the past few years. So, when we talk about memories the immediate type of memory that comes to our mind is the SRAM cell because they are fast in operation, easy to implement on a larger scale, can be overwritten easily etc. But one thing that affects their performance is the NBTI. NBTI has been there for ages this paper explains NBTI in detail, their effects on the performance of the SRAM cells and a recovery method to overcome it.

II. FORMATION OF Si-H BONDS

A basic PMOS device consists of an n-type substrate or bulk on top which we have the oxide layer and the gate terminal. Adjacent to these are the p-type drain and the p-type source terminals.

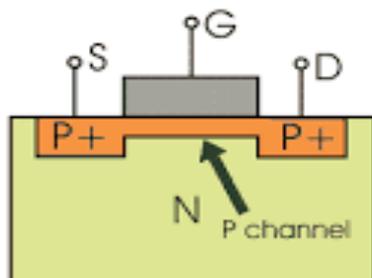


Fig. 1 Basic structure of a PMOS device

The fabrication is done in such a way that a new process called hydrogenation is introduced immediately after the oxidation process. Because of this hydrogenation, the hydrogen atoms from weak bonds with the silicon atoms in the lattice. The silicon atoms stay in their lattice positions as such and the hydrogen atoms get surrounded around them.

Now, how a PMOS device operates will be the next question. The process is very simple. A high positive bias is applied to the source terminal of the n-type substrate. The holes in the source tend to repel

away from the positive charge contained in the positive bias and move into the substrate region. The holes get accumulated right below the interface or the surface between the oxide layer and the substrate. This region is called as the inversion channel or the inversion layer. It is called as the inversion channel because it consists of holes whose charge is opposite to the charge of the electrons contained in the substrate. Thus a PMOS device is fabricated.

III. INTERFACE TRAP

Now these holes in the inversion channel move with a high energy at a great velocity of the order of 10^6 m/s from the source terminal to the drain terminal when a strong negative bias is applied to the gate terminal of the device. So, as and when they move, they collide with each other and with the silicon atoms in the lattice to reach the drain terminal. Only when this happens, the drain current actually flows from the drain to the source.

However, during this process the holes tend to interact with the weak Si-H atoms and break them apart. As a result, the H atoms get separated and move towards the oxide layer. These H atoms get accumulated in the oxide layer but there is a small proportion of the H atoms getting deposited right at the interface or the surface between the oxide layer and the inversion channel. Now, these H atoms at the surface act as defects.

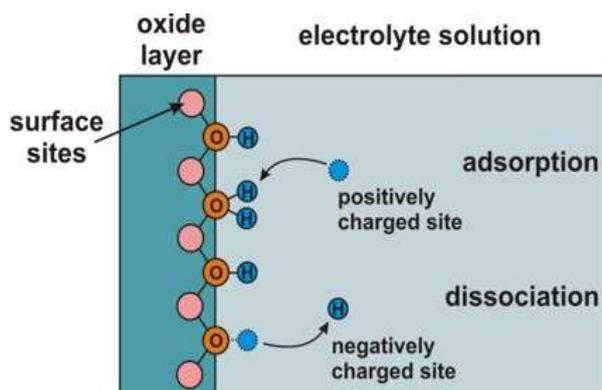


Fig. 2 Process of formation and dissociation of the hydrogen atoms from the silicon atoms.

These defects trap the holes that are moving freely in the inversion channel and contribute to the less number of holes moving from the source terminal to the drain terminal. This trapping of the holes at the interface due to the defects thus formed is what is called as the interface trap.

IV. EFFECTS OF NBTI

Now due to this negative bias at the gate, majority of the hydrogen atoms get accumulated in the oxide layer giving rise to an increased oxide thickness and an increase in the overall charge enclosed within the oxide layer. Due to this increase in the oxide thickness, the overall oxide capacitance decreases following the equation

$$C_{ox} = \epsilon_{ox} / t_{ox} \quad (1)$$

Where

C_{ox} is the oxide capacitance

ϵ_{ox} is the permittivity of the oxide layer

t_{ox} is the oxide thickness

This decrease in the oxide capacitance and the increase in the charge contained in the oxide layer together lead to an increase in the voltage across the oxide layer. This is explained by

$$V_{ox} = Q_{ox} / C_{ox} \quad (2)$$

Where

V_{ox} is the voltage across the oxide layer

Q_{ox} is the charge enclosed within the oxide layer

C_{ox} is the oxide capacitance

Every MOSFET device will have its own threshold voltage beyond which it actually conducts.

This threshold voltage is given by the formula

$$V_t = V_{fb} + 2\psi_B + V_{ox} \quad (3)$$

Where

V_t is the threshold voltage

V_{fb} is the flat band voltage

ψ_B is the bulk potential

V_{ox} is the potential across the oxide layer

Now this increase in the voltage across the oxide layer increases the threshold voltage of the device under operation. This increase in the threshold

voltage and the decrease in the oxide capacitance in turn decreases the drain current of the PMOS device. The drain current equation that is most commonly used is

$$I_d = (1/2) * (\mu_n C_{ox} (W/L) (V_{GS} - V_{th})^2) \quad (4)$$

Where

V_{th} is the threshold voltage.

C_{ox} is the oxide capacitance.

μ_n is the mobility of the charge carriers.

V_{GS} is the gate to source voltage.

I_d is the drain current or the drive current.

W/L is the width to length ratio of the MOSFET device.

This drain (drive) current of the device is responsible for the performance of the transistors in terms of speed of operation. If the drive current is less the device operates slower and if the drive current is more the device operates faster.

Thus, we can infer that the strong negative bias applied at the gate terminal, causes a gradual shift in the threshold voltage of the device thus giving rise to a decreased drain current flowing in the device affecting the performance badly.

Now let us see how NBTI bothers the behavior of a simple 6T SRAM cell and affects its performance.

V. 6T SRAM CELL AND THE EFFECT OF NBTI

A basic 6T SRAM cell is shown in the Fig. 3 with the different lines 'WL' and 'BL'-'/BL' for the write and the read operations. The lines 'WL', 'BL' and '/BL' are all used for the basic read and write operations of the SRAM cell.

In the read operation, the data is read from the cell using the bit lines 'BL' and '/BL' and the value that is read is detected with the help of a sense amplifier. The sense amplifier senses the difference in the voltage levels between the bit lines 'BL' and '/BL' to detect if there was a '0' or a '1' stored in the cell. In the write operation the value is just written to the cell using the bit lines 'BL'-'/BL' and the write line 'WL'.

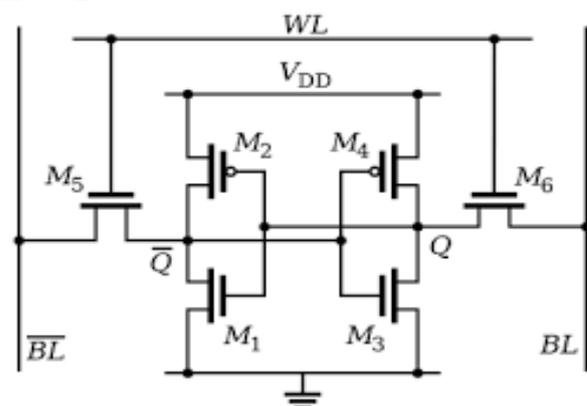


Fig. 3 Basic 6T SRAM cell

There is also the third mode that the cell operates in called the 'Standby' mode where the SRAM cell just holds the data that was written earlier until the next write operation is performed. In this circuit, say for instance the node '/Q' holds a value of '0' and the node 'Q' holds a '1', then the input to the PMOS transistor 'M4' is a '0' and the input to the NMOS transistor 'M1' is a '1'. This means that the PMOS transistor is said to undergo the effect of NBTI and the NMOS transistor to undergo the effect of PBTI where PBTI stands for Positive Bias Temperature Instability. PBTI is similar and opposite to NBTI as it is caused due to the positive bias applied on the gate of the NMOS transistor.

A similar effect takes place wherein the PMOS transistor 'M2' undergoes NBTI and the NMOS transistors 'M3' undergoes PBTI had the values stored in the nodes '/Q' and 'Q' been a '1' and '0' respectively. We say that the transistors are affected by NBTI (for PMOS) and PBTI (for NMOS) because of the fact that the drive currents of these transistors are lowered which leads to reduced performance in terms of speed and accuracy of operation.

VI. LEAKAGE CURRENT

Any circuit if we consider will have a small amount of current flowing inside even if the circuit is completely switched off. This current is called as the leakage current. Leakage current is something that persists for ages and it is still an important factor researchers, designers and developers are trying to mitigate as it might affect the performance and reliability of the circuit or the device on a larger perspective.

Equations (1), (2), (3) and (4) as referenced from 'Fundamentals of MODERN VLSI DEVICES, Taur & Ning, Cambridge Univ. Press, 1998. (ISBN 0 521 55056 4); 2nd ed., 2009'

Leakage current is normally determined by switching ON the power supply to the circuit while applying a zero bias on the gates of the transistors so that they are completely turned OFF. The leakage current in this case is the current that flows from the supply voltage to the ground. Ideally there should not be any current flowing in the circuit but practically you can find a small amount of current flowing in the order of mA, μ A, nA, fA etc. depending on the scaling and the sizing factors.

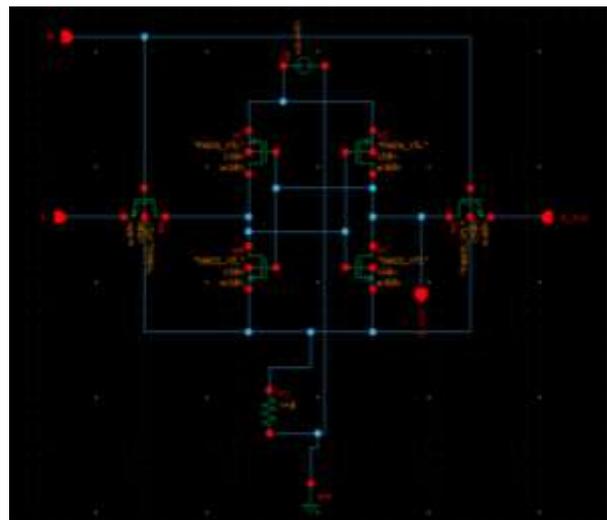


Fig.4(a) Circuit to analyze the leakage current of the conventional cell

With regards to the 6T SRAM cell that is considered in this paper, the leakage current is normally determined by making the write line 'WL' and the bit lines 'BL'-'/BL' go LOW ('0'). This way you can completely switch OFF the cross-coupled inverters and hence the entire circuit under consideration. However, you will have to switch ON the supply voltage to determine the amount of current flowing in the circuit from the supply to the ground.

As referenced from 'Enhancing NBTI Recovery in SRAM Arrays Through Recovery Boosting - Taniya Siddiqua and Sudhanva Gurumurthi - IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 4, APRIL 2012' this paper has proposed a modified 6T SRAM cell that is used to minimize the amount of leakage current flowing in the circuit. It uses a pair of sleep transistors (2 PMOS transistors) and an external control signal 'con'. The modified 6T SRAM cell is shown in the Fig.4 (b).

The sleep transistors are used for power gating. Power gating means that the gate of the cell/ circuit is driven by a transistor which acts as the virtual V_{DD} or gnd. So, eventually if the supply voltage to the circuit is reduced then the amount of leakage current flowing is also reduced. Here, in our design, the PMOS sleep transistors are used and they act as virtual V_{DD} thus reducing leakage. PMOS transistors are used as sleep transistors because they are said to have better leakage characteristics than the NMOS transistors.

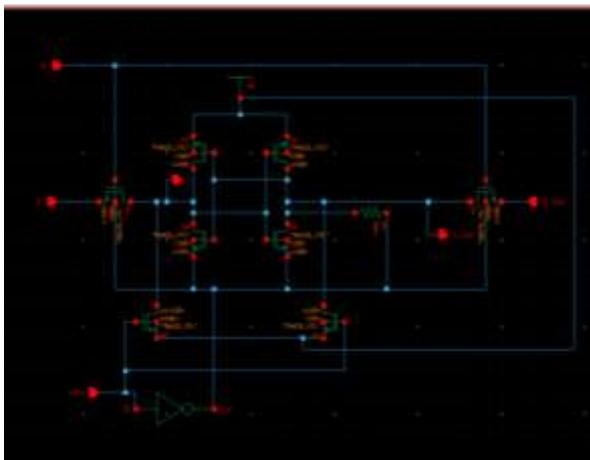


Fig.4 (b) Schematic representation of a modified 6T SRAM cell

In the PMOS sleep transistors one terminal is connected to a V_{DD} rail and the other end is connected to the nodes 'Node0' and 'Node1' respectively. The gate input to these two PMOS transistors is given with a control signal 'con' whose value is controlled externally. The 'con' input has an inverter connected to it which connects the cross-coupled inverters to the ground rail. If the value fed to the 'con' input is a '1', then the cross-coupled inverters are connected to the ground rail (a LOW '0'). Also, since the value fed to the gate inputs of the two additional PMOS transistors is a HIGH ('1'), the transistors are completely switched OFF. Thus the SRAM cell operates as expected in the conventional mode.

However, if the value fed to the 'con' input is a LOW ('0'), then the cross-coupled inverters are connected to the ground rail whose value is gradually increased from LOW ('0') to HIGH ('1'). Also, since the value fed to the gate inputs of the two additional PMOS transistors is a LOW ('0'), the PMOS transistors are switched ON and hence the nodes 'Node0' and 'Node1' go HIGH ('1'). Thus, the SRAM cell is said to operate in the recovery mode and experiences less NBTI while producing the desired output.

VII. IMPROVED READ STABILITY AND WRITE ABILITY

The circuit shown in Fig.5 consists of two additional NMOS transistors connected in the pull-down network of the conventional 6T SRAM cell. By adding additional NMOS transistors, the strength of the pull-down network is increased which plays an important role. It is said that if the strength of the pull-down network is more than the strength of the pull-up network then eventually, that will help the cell to perform a better read operation. The circuit is designed in a similar way with two external signals 'x' and 'y' as inputs to these additional NMOS

transistors. The N-curve characteristics for this circuit will be explained in the later part of the next section.

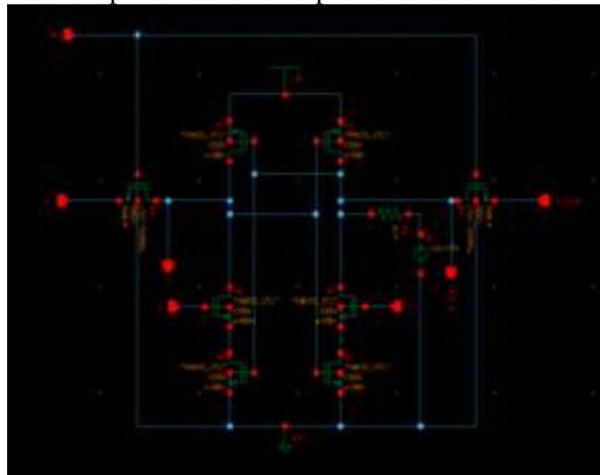


Fig.5 Improved circuit to determine the write ability and read stability

VIII. SIMULATION AND RESULTS

The circuit designs were based on the GPDK45 technology and the simulations were performed using Cadence. The transistors that were used in the design were based on the 45nm submicron technology with default threshold voltage values. Transient analysis and DC analysis were performed on the designed circuits in order to get the waveforms, leakage dependency and the N-curve.

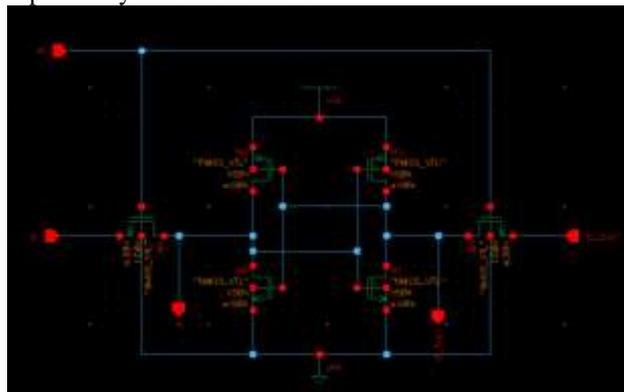


Fig.6 (a) Basic 6T SRAM cell

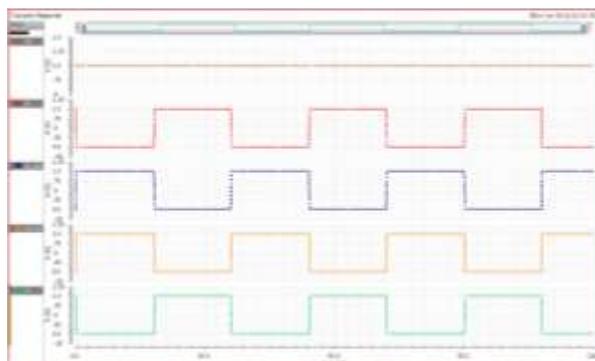


Fig.6 (b) Waveform representing the basic read/ write operation of a conventional 6T SRAM cell.

Fig.6 (a) and (b) show the schematic representation of a conventional 6T SRAM and the waveform that describes the basic read/ write operations respectively.

Fig.7 depicts the circuit that was used to determine the read/ write currents of the conventional type 6TSRAM cell. Fig. 7 (a) gives us the read current that is defined as the amount of current required by the conventional 6T SRAM cell to perform a stable read operation. Similarly, Fig.7 (b) gives a measure of the write current required by the conventional SRAM cell to perform a write operation.

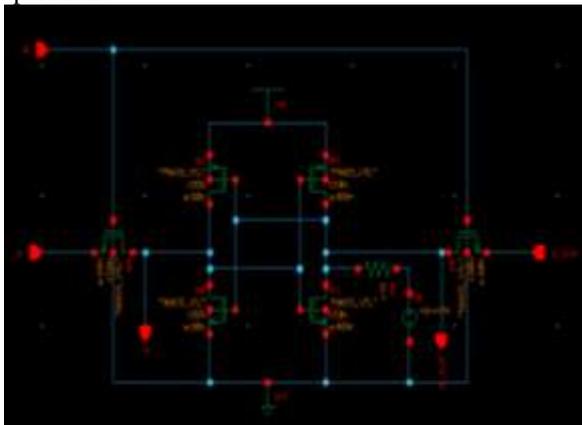


Fig.7 Schematic representation of the conventional 6T SRAM cell to determine the read/ write currents.

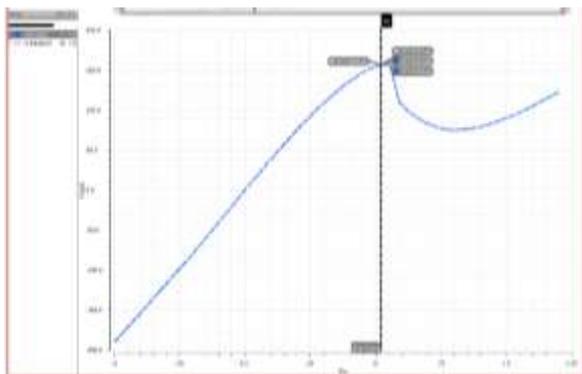


Fig.7 (a) Read current depicting the read stability

Fig.4 (a) shows the circuit that is used to detect the leakage current flowing in the conventional cell as discussed earlier in section VI. Fig.8 (a) shows the dependency of the leakage current on decreasing V_{DD} for this conventional cell. As you could see, the current decreases from $37 \mu A$ to $0A$ as the voltage is swept from 1V to 0V. However, Fig.8 (b) shows how the leakage current in the modified 6TSRAM cell (as depicted in Fig.4 (b)) varies with respect to a decreasing supply voltage V_{DD} from 1V to 0V. We can see that the leakage current using the modified circuit in Fig.4 is decreased to near $13 \mu A$ which is $1/3^{rd}$ of the leakage current found in the conventional 6TSRAM cell (Fig.8 (a)).

The circuit shown in Fig.4 (b) apart from dealing with leakage, also deals with NBTI. The circuit as you can see uses the external control signal 'con' that is actually controlled to switch the 6T SRAM cell between the conventional mode and the recovery mode. It is called the recovery mode because the PMOS transistors are maintained at logic '1' so that they do not undergo the effect of NBTI.

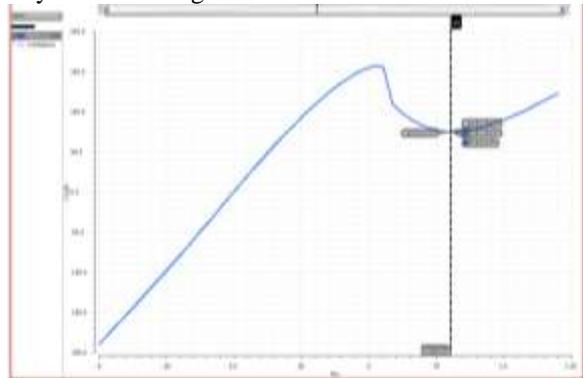


Fig.7 (b) Write current depicting the write ability

It is important to switch between the normal mode and the recovery mode because when you take a big architecture consisting of an array of SRAM cells, if we would want read from or write to a particular SRAM cell, the other cells connected in the array are also affected. This is because, the 'BL' and the 'BLB' lines are connected to the SRAM cells in the array as they are arranged in the row-column fashion. So if we want to read from or write to a particular cell, the values in the 'BL' and 'BLB' lines keep changing continuously.

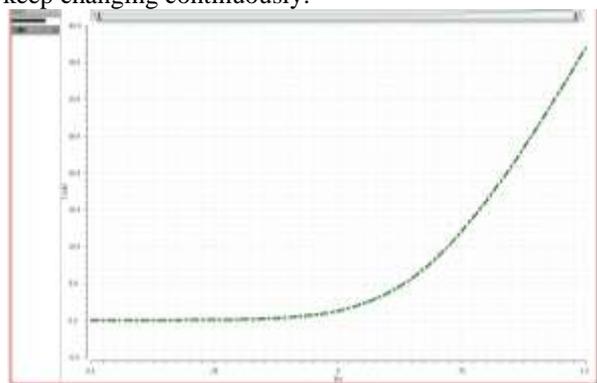


Fig.8 (a) Leakage current of the conventional cell

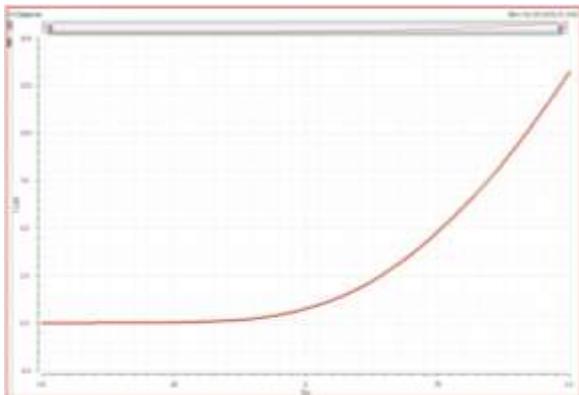


Fig.8 (b) Leakage current of the modified cell in Fig.4

Because of this, the cells undergo NBTI and if we have the 'BL' and 'BLB' lines to be connected to every cell in the array, then we have every cell to undergo NBTI which is undesirable. It is therefore important to isolate the other SRAM cells that are not in use and just use the cell that want to read the data from or write the data to.

During this process, when we have the 'con' signal to have the value '1', the cell is said to be operated in the normal conventional mode and when we have the 'con' to hold a value of '0', then we say that the SRAM cell is said to be in the recovery mode. The waveforms in the Fig.9 (a) and (b) describes the operation modes (normal mode and recovery mode) of the modified 6T SRAM cell.

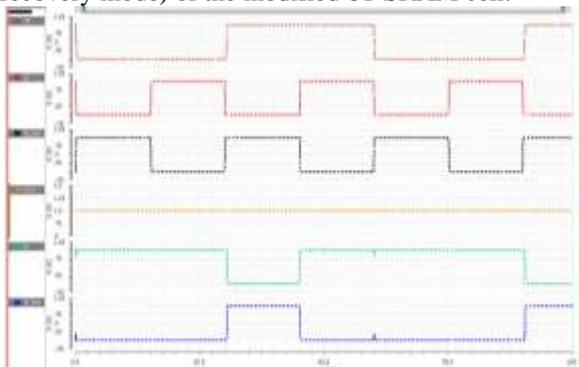


Fig.9 (a) Waveform showing the 6T SRAM cell operating in the conventional mode with 'con'=1

One thing to be noticed here is that the additional PMOS sleep transistors added to the circuit have high threshold voltages. In the normal mode when the 'con' is 1, the PMOS sleep transistors are OFF and only when the 'con' is 0, the sleep transistors are ON. However, as we know the 'con' signal will not be at 0 for a long time and since we have a higher V_{th} , this makes them immune to the NBTI effect and does not undergo any degradation.

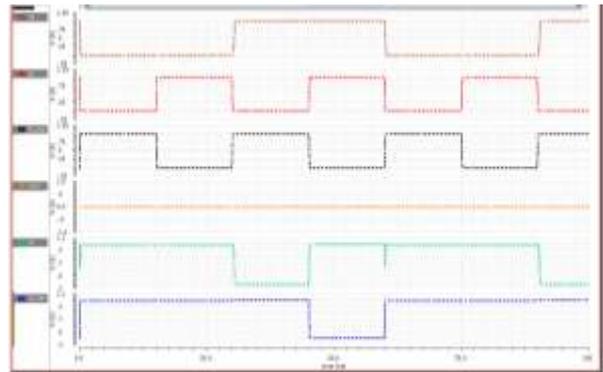


Fig.9 (b) Waveform showing the 6T SRAM cell operating in the recovery mode with 'con'=0

The improved circuit uses two additional NMOS transistors connected in series to the already existing NMOS transistors with the default threshold voltage values. The input was fed externally using pins 'x' and 'y'. A circuit similar to that of the conventional 6T SRAM cell depicted in Fig.7 is designed and similar simulations are performed in order to obtain the N-curve.

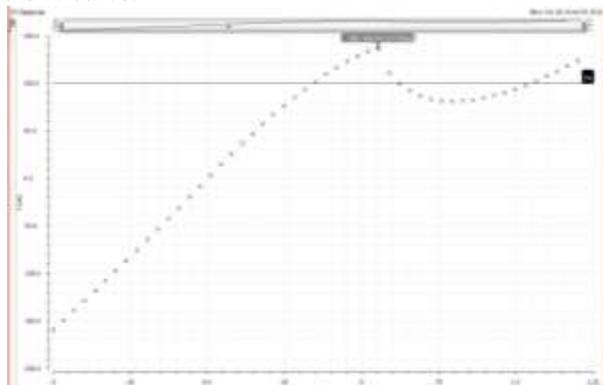


Fig.10 (a) The N-curve of the improved circuit in Fig.5 showing the read current

The waveforms in the Fig.10 (a) and (b) give us the N-curve that is required to measure the read and write currents. It is quite obvious from the values of the read and write currents obtained from these waveforms that we could achieve a better read stability and write ability. The N-curve depicted by the improved circuit in Fig.5 shows a better waveform or in other words improves the read stability and write ability in comparison to that of the currents measured by the conventional 6T SRAM cell. The comparison is presented in the form of a table in Table.1.

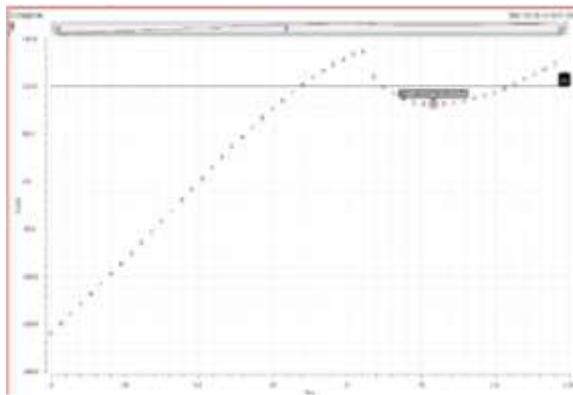


Fig.10 (b) The N-curve of the improved circuit in Fig.5 showing the write current

	Conventional 6T SRAM cell	Improved 6T SRAM cell (Fig. 5)
SVNM	350.518 mV	288.257 mV
SINM (Read Stability)	57.0485 μA	37.05 μA
WTV	448.8160 mV	414.717 mV
WTI (Write Ability)	-25.0207 μA	-18.69 μA
Leakage Current	37 μA	13 μA

Table.1 Comparison of the Read stability and write ability between the conventional 6T SRAM cell and the improved circuit as in Fig.5

IX. CONCLUSION

The effect of NBTI on the SRAM cells have been there for ages and there are different research works being performed to analyze ways to overcome it. The methods prescribed in this paper to overcome the effect of NBTI are vital and proved using simulations and designs. This paper also talks about leakage that is considered to be one of the important problems in field of memories and also compares it with the conventional cell.

A number of research papers are available on ways to overcome both NBTI and PBTI at both architectural level and design level/ circuit level. But, implementing it at the architectural level would need knowledge on microprocessors, cache memory and the different principle algorithms involved. Since NBTI happens at a device level and hence changes the device parameters such as the oxide thickness, threshold voltage, drive current, it becomes certainly impossible to completely eliminate the effects of NBTI at the device level. However, consistent efforts are being made to lessen the effect of NBTI on the

SRAM cells at the architectural level as there follows a series of variations at the device level.

As and when scaling happens, the effect of NBTI increases on the SRAM cells and it is found that the device variations increases in proportion. So, this is something that will affect the future of the MOSFETs and it is studied that different methods may be performed in the trial and error basis in order to overcome the effect of NBTI.

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